# A broadband PLC communication system in C band

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**Abstract**

Telecommunication companies offer customers new home services which requires new physical mediums of transmission but addition of wires is not a desired solution. Last years, new technologies have been developed in order to solve this problem of signal distribution like home-plug and home-rf. This work present a communications system based on PLC using the free C band between 100 kHz and 500 kHz. Its main objective is implementation of a low cost full digital modem using advanced digital technology capable of support voice and data communications and QoS assured. In this work we will present the design co-simulation process using software tools as system generator, Simulink and ISE, and hardware evaluation board.

## 1. Introduction

### 1.1. Power-line channel

In time domain [3], power-line channels can be observed as an infinite number of multi-paths due to direct multi-path and reflections at the line junctions and appliances. Another important effect is impulsive noise which generates busts errors in data transmission. Main characteristics of power-line channels in frequency domain [4] are presence of deep notches, great variation of the attenuation with frequency and high dispersion of the amplitude value among channels.

### 1.2. OFDM

In an OFDM system [1], data is carried on narrow-band sub-carriers in frequency domain using the IFFT/FFT transform at the transmitter/receiver respectively. The number of points of this transform translates into the total number of orthogonal sub-carriers and the samples after each IFFT calculation are named symbol OFDM.
Part of this symbol is replicated from the back to the front in order to create a guard period (cyclic prefix) [2] used to combat the ISI and ICI introduced by the multi-path channel through which the signal is propagated. If the duration of the cyclic prefix is choose longer than the worst-case delay spread of the channel, there is no ISI since the previous symbol, only have effect over samples into the guard period which will be discarded and there is no ICI because the samples selected encompass the contribution from all the multi-path components.

## 2. System parameters

| | | |
|---|---|---|
| BW | Bandwidth | 400 kHz |
| Δf | Sub-carrier frequency spacing | 6.25 kHz |
| Tfft | FFT/IFFT period | 160 μs 64 Chips |
| Tgi | Cyclic prefix | 10μs 4 Chips |
| Tsym | Symbol interval | 170 μs 68 Chips |
| Nsd | Number of data sub-carriers | 48 |
| Nsp | Number of pilot sub-carriers | 4 |
| Ns | Number of sub-carriers, total | 64 |
| Nbpsc | Coded bits per sub-carrier (16-QAM) | 4 |
| Ncbps | Coded bits per OFDM symbol | 192 |
| Ndbps | Data bits per OFDM symbol | 96 |
| | Convolutional rate | 1/2, 2/3, 3/4, 1 |
| | Reed-Solomon rate | 28/32, 1 |
| C | Coding rate total (worst and best case) | 7/16, 1 |
| Rwc | Data rate, total (worst case) | 494 kbps |
| Rbc | Data rate, total (best case) | 1129.4 kbps |

The system is operating in the CENELEC band between 100 kHz and 500 kHz which a total bandwidth of 400 kHz. The architecture of the system is based in the 802.11a standard and it also uses 64-point FFT and the total OFDM frame duration is 68 chips where 64 are for data and 4 are for

cyclic prefix. Notice that in 802.11a standard 16 chips are used in the cyclic prefix which translates in a guard time of 0.8µs, but now 4 chips have a duration of 10 µs which is larger than the worst-case delay-spread in PLC. With this the system efficiency is increased from 4/5 to 17/16. Out of the 64 narrow-band sub-carriers, 52 are used for data and 16 are zeros.

Four of the 52 sub-carriers are used as pilot signals for channel estimation and other 48 are used for data transporting each one 4 bits with a 16 QAM modulation scheme.

Due to noise introduced by power line environment a coding channel block is needed to improve the BER. It is implemented using two stages: one internal and another external. The internal encoder is used to correct random errors due to white noise and is a convolutional code with Viterbi decoder and rate 1/2. Proper puncture can be applied to this code to obtain rates of 1, 2/3, 3/4 improving the throughput when channel allow it.

On the other hand impulsive noise present in power line channel create bursts errors which cannot be corrected using a Viterbi decoder, then the system includes a Reed-Solomon encoder which has optimal performance in burst error correction. The RS selected is the shortened code 28-32 which can correct burst frames up to 1µs (typical in power line channels) after an adequate interleaving.

The total data rate we can achieve depending on the code scheme used varies between 494 kbps and 1129 kbps.

## 3. Implementation

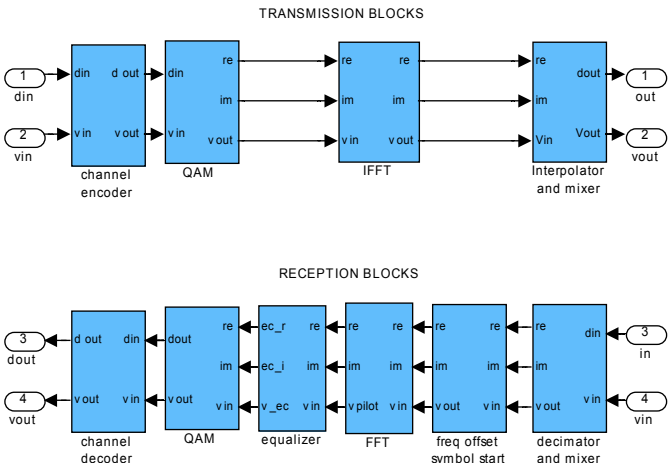


**Figure 1.** Block diagram.

System Generator under Symulink platform has been used to design and simulate the model. Figure 1 shows the block diagram where we can see the transmission and reception stages. In the transmission way we can see a first stage of channel encoding (RS encoder, convolutional encoder and interleaving blocks), an OFDM with 16 QAM modulation systems and finally the stages of interpolation and mixing to obtain a 20 MSPS with 12 bits of precision signal to attack the DA converter.

On the other hand a 20 MSPS is provided by AD block as input to digital decimator and mixing blocks. Before FFT block a stage for frequency offset estimation and correction is needed to guaranty the sub carriers orthogonally. Besides, this block calculates the start of each OFDM symbol and removes the cyclic prefix. When the 48 sub carriers of data are discomposed using the FFT algorithm, they are passed through an equalizer and a 16 QAM demodulator. Finally, we can see the channel decoder stage composed of Viterbi and RS blocks with interleaving stages used for error correction.

The system has been synthesized to hardware running at 40 MHz clock frequency into the Virtex 1000E FPGA without including de Viterbi and RS blocks.

## 4. System evaluation

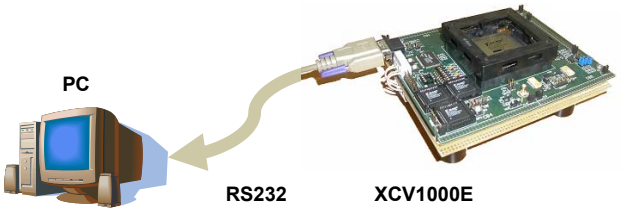


**Figure 2.** Evaluation scheme.

In order to test the system previously to be connected to power line we using a cosimulation process combining software and hardware simulation. Figure 2 shows the evaluation schema where the core of the system was be combine with a serial interface and a digital setting channel models. The model of Figure 3 was bee implemented in an evaluation board and connected by a serial link to a PC running the model of Figure 4.

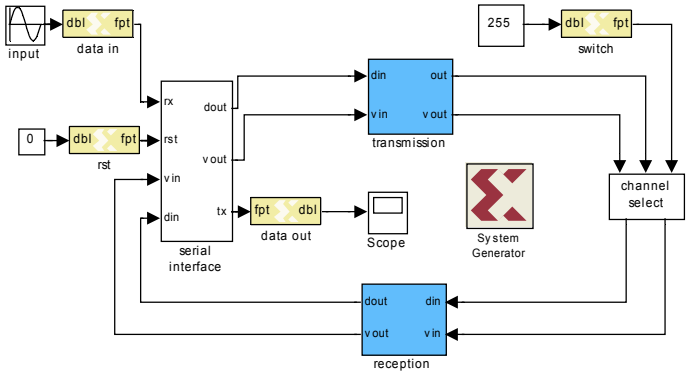


**Figure 3.** Evaluation hardware system.

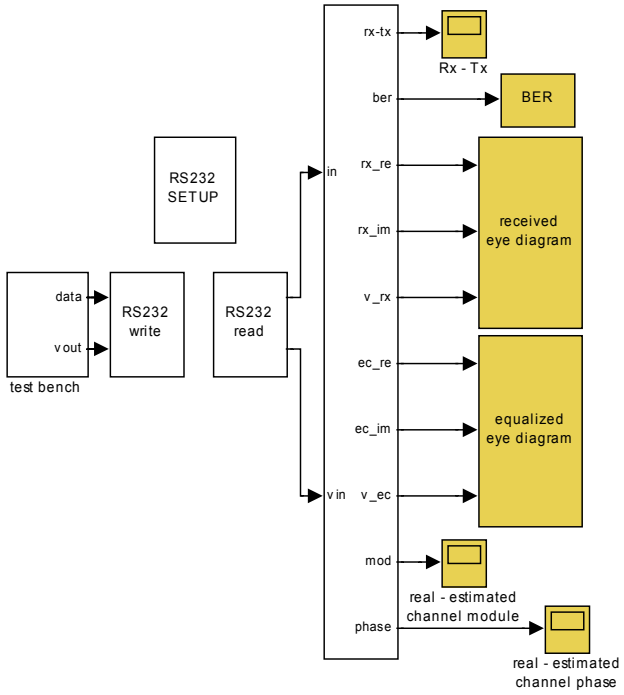


**Figure 4.** Simulink test bench.

The Figure 4 show the Simulink test bench used to evaluate the system. The test bench bock provide to the hardware the frames to transmit using a serial interface. The serial reads interface read the real output of the hardware. Finally the read information is displayed in different types of diagrams.

**Figure 5.** Evaluation board.

The hardware design has been tested using an evaluation board ADD7100 (Figure 5) with a Xilinx Virtex 1000E FPGA. The ADD7100 board includes ZBT RAM, static RAM, FLASTH, 4x32x2 I/O configurable pins, a mixed signal front end (MxFE) to power line and a serial interface for PC-Board communication as Figure 2 shows.

System response has been tested under different channel models using this board and the model of Figure 3. First channel test is "no channel". Figure 5.1 shows the linear phase in frequency introduced by FIR filter blocks and how the equalization stage can estimate it accurately. In Figure 5.2 we can see as the global signal spectrum is flat in frequency and Figure 5.3 and 5.4 are the eye diagram of pre and post equalized received signal respectively, obviously under this conditions all QAM symbols are decoded correctly.

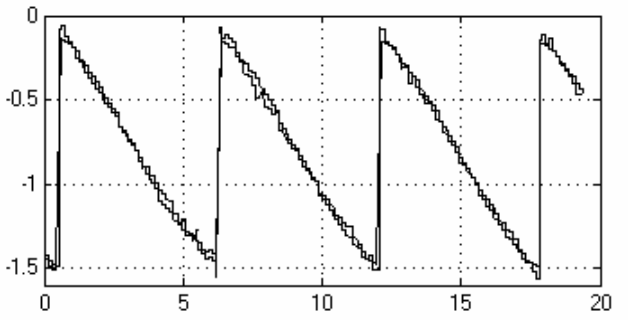


**Figure 5.1.** Real and estimated phase channel.

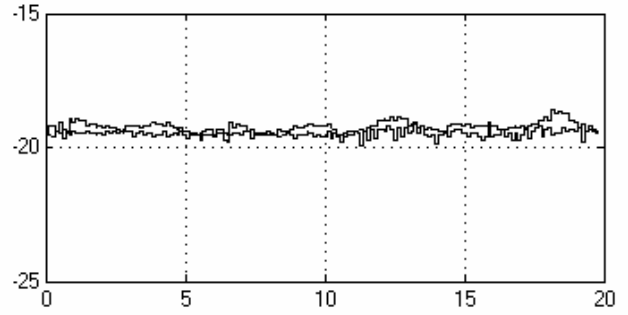


**Figure 5.2.** Real and estimated module channel.

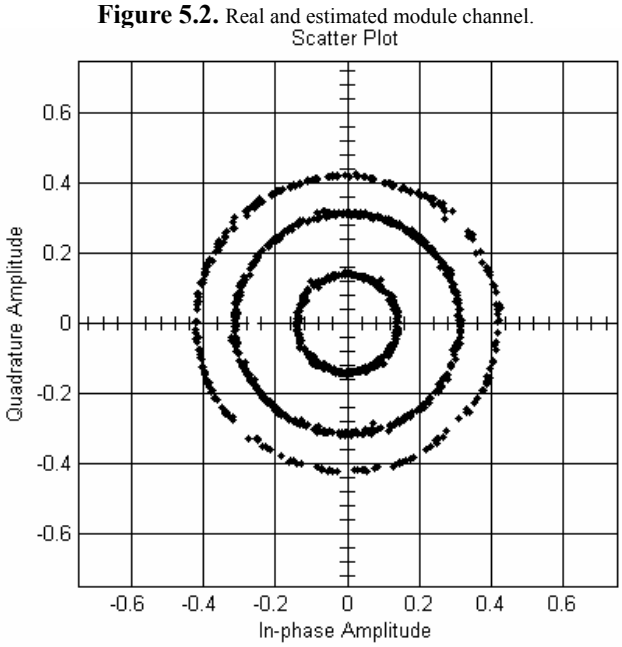


**Figure 5.3.** Received eye diagram.

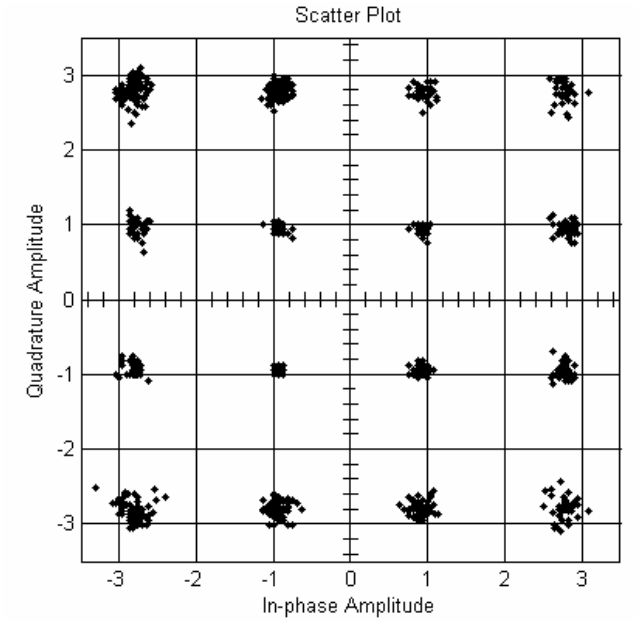


**Figure 5.4.** Equalized eye diagram.

In the second step, we introduce a Gaussian noise channel, this model consist of reducing the precision bits in the AD and DA converters (characteristics presented in [5] are supposed for AD DA blocks). When precision is reduced from 12 to 6 bits some received samples are nearest the eye diagram decision boundaries producing a BER of 0.0001.

Another important impairment to be tested is impulsive noise. Under this conditions the equalization block can do nothing to stop the burst error received but the LMS based estimation block try to readapt its coefficients and when this noise disappear this block need some time to return the optimal state so the effect is increased. A BER of 0.048 is registered when impulsive noise is 5% present in time. This BER do not include the Viterbi and RS blocks with interleaving stages used for error correction that can support this error rate widely.

In thirst step to evaluate the frequency dependent attenuation we introduce in the channel model an IIR filter which produces a nonlinear phase and large attenuation variations in the signal band. The system's equalizer offers a great performance considering that only 4 pilot samples of channel are used to calculate the 48 others. Only a BER of 0.0004 is received under these conditions.

Finally we evaluate a real case in which all impairment effects are included in the channel model. Figure 6.1 and 6.2 show 4 consecutive channel estimations when it's reached the optimal state. In Figure 6.3 and 6.4 it's displayed the eye diagram received and equalized respectively, where we can see the errors caused by impulsive noise. The transmitted and received data sequences (an 8 bit coded sin wave in this example) are shown by Figure 6.5. Burst errors due to impulsive noise and random errors due to Gaussian noise and inaccurate estimation of channel can be seen in it. The BER in this case is increased up to 0.05 but correction blocks can support this error rate widely.

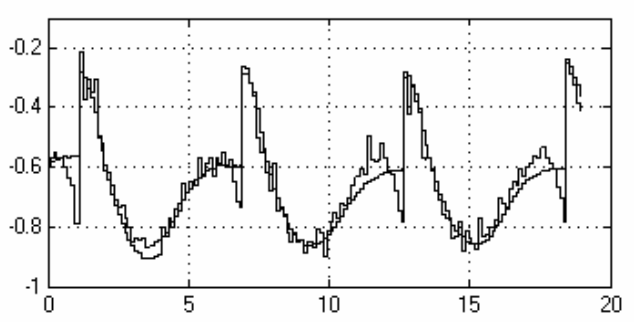

**Figure 6.1.** Real and estimated phase channel.

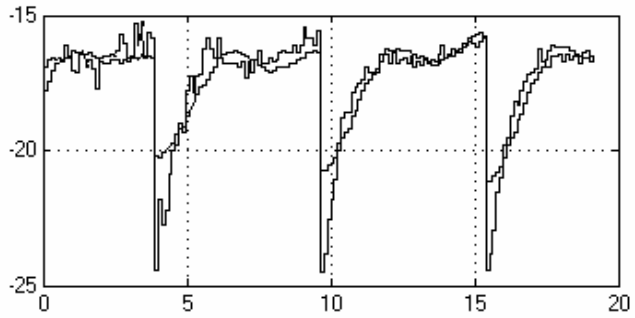

**Figure 6.2.** Real and estimated module channel.

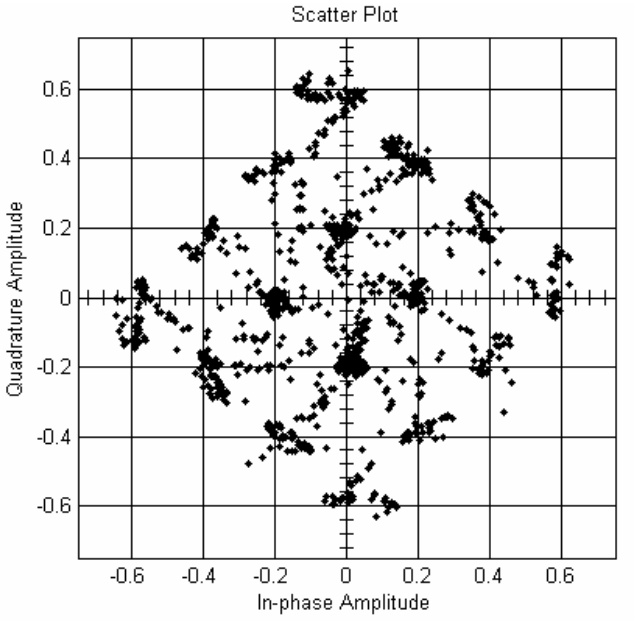


**Figure 6.3.** Received eye diagram.

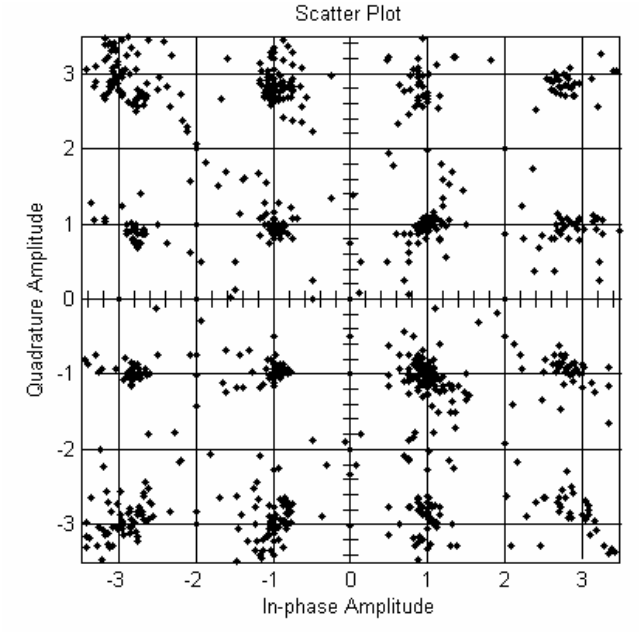


**Figure 6.4.** Equalized eye diagram.

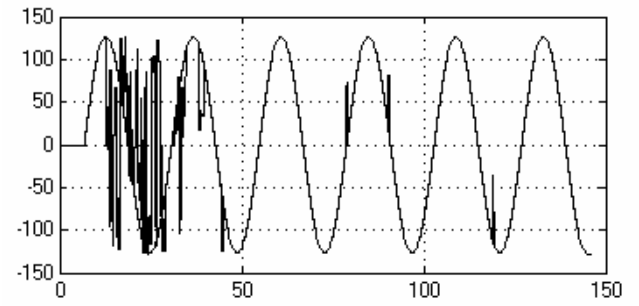


**Figure 6.5.** Transmitted and received data.

## 5. Conclusions

A broadband PLC communication system in CENELEC band using OFDM techniques has been implemented and tested under different channel models which simulate the power line environment. Test shows a very good performance of LMS based equalization system under channels with nonlinear phase and great attenuation variations in the signal spectrum and time varying response. Co-simulation using system generator, Simulink and VHDL modules have been presented as a new and interesting procedure for hardware design.

## References

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